REMARKS/ARGUMENTS

Claims 1-22 are pending in the application. Reconsideration in view the following remarks is respectfully requested.

The Office Action objects to the Title and Claims 6 and 9-10. The Office Action rejects claims 1-22 under 35 U.S.C. 102(b) as being anticipated by Yeager et al. (U.S. Patent No. 5,758,112). Applicants are amending the title of the invention as requested by the Office Action. Claims 6 and 9 are amended for clarification purposes to overcome any objections as well. Claim 15 is cancelled without prejudice or disclaimer.

Applicants respectfully submit that none of the cited sections of Yeager teach, suggest or reflect at least a processor, comprising a physical register file populated by a number of registers, an instruction decoder, a register alias table coupled to the instruction decoder, an active list populated by a number of entries, the entries include an old field and a new field, and a free list of unallocated physical registers reclaimed from said active list as recited in claim 1.

The cited reference Yeager does not contain such limitations anywhere in its disclosure. The Office Action states the limitation an active list (212) populated by a number of entries, the entries include an old field and a new field can be found at col. 15 lines 38-54 and elements 282 and 256. Column 15 lines 38-54 states:

> "Active list 212 contains an ordered list of all active instructions. An instruction becomes active after it has been decoded. It remains active until it graduates (completes in program order) or is aborted by reversed branch decision or an exception. When an instruction with an exception graduates, all subsequent instructions are flushed from the pipeline. Active list 212 is emptied in reverse order. For each instruction, the logical register is renamed to its previous physical register, and its new physical register is returned to the free list. Active list 212 is implemented as a 32-word circular FIFO, whose structure is similar to free lists 208 and 210. Like the free lists, active list 212 consists of four eight-entry RAM memories. Four consecutive entries can be written (during decode) or read (during

graduation) by accessing one entry in each memory. "

Also, element 256 is designated in Yaeger as a "logical destination registration number" and element 282 is designated as a "old physical destination".

Applicants' respectfully submit neither of the cited section disclose, teach or suggest "...an active list populated by a number of entries, the entries include an old field and a new field" as recited in claim 1. The Office Action asserts that the "new field" limitation of the equivalent of the logical destination registration number 256 of Yeager. However, this is not the case and the operation of the logical destination registration number 256 indicates so. Column 7 lines 40-44 of Yeager state: "Conversely, logical destination register number 256 is mapped to a physical destination register number held in integer free list 210, as shown by line 270, resulting in a physical register number 272 (Dest)". The function of the logical destination register number 256 in Yeager is functionally dissimilar to that of the new field in an embodiment of Applicants' invention. Support can be found at least at page 6 line 27, and page 7 line 24 of the Specification.

Therefore, since at least the limitation "new field" is not taught or suggested anywhere in the Yeager reference, independent claim 1 is in condition for allowance and the 35 U.S.C. 102(b) rejection should be withdrawn. Independent claims 8 and 19 include similar limitations and are in condition for allowance and the 35 U.S.C. 102(b) rejection should be withdrawn. Claims 2-7, 9-12, 20-22 depend from allowable independent claims 8 and 19 and therefore are allowable also.

Applicants respectfully submit that Yeager does not disclose a method for recovering registers in a processor, comprising reading a bit in an active list, reclaiming a physical register from said active list to a free list according to said bit; and setting said bit during a misprediction condition as described in amended claim 13.

The cited reference Yeager does not contain such limitations anywhere in its disclosure. The Office Action states the limitation "further comprising setting said bit during a misprediction condition" can be found at column 17 lines 26-50 which states:

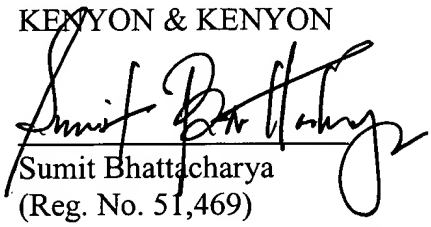
> "[a]s discussed above, redundant mapping tables 204' and 206' (FIGS. 3-7) make a copy of mapping tables 204 and 206, respectively, for use if a branch is restored. Although processor 100 decodes up to four instructions in parallel, mapping tables 204 and 206, in their preferred embodiment, are not updated for each instruction individually. Rather, these tables make a copy at the beginning of the decode cycle (i.e., stage 2). Thus, the precise restore point for a particular branch instruction might not exist in redundant mapping tables 204' and 206'. As such, the changes made during the cycle are recorded separately in branch stack 216. That is, the destination registers of the four instructions decoded during the same cycle are saved in the branch stack. If all four instructions are decoded in a single cycle, an alternative embodiment of redundant mapping tables 204' and 206' could make a new copy of mapping tables 204 and 206, respectively, during the following cycle. This embodiment would eliminate the need for saving the fourth destination register. However, this extra redundant mapping operation might coincide with a redundant mapping operation for a second branch instruction. To accommodate simultaneous redundant mapping operations, stronger drivers would be required to accommodate simultaneous writes to redundant RAM cells".

These cited sections of the Yeager disclose the operation of the "redundant mapping tables", whose operation and function do not at all reflect the limitation of "setting said bit during a misprediction condition" as disclosed in Applicants' invention. Therefore, since these cited sections in no way reflect the limitations and operations of setting said bit during a misprediction condition as disclosed in Applicants' invention, independent claim 13 is in condition for allowance. Claims 14 and 16-18 depend from allowable independent claim 13, and therefore are in condition for allowance as well. For at least the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON

Dated: March 3, 2004 By: 

Sumit Bhattacharya
(Reg. No. 51,469)
Attorneys for Intel Corporation

KENYON & KENYON
333 W. San Carlos St., Suite 600
San Jose, CA 95110
Telephone: (408) 975-7500
Facsimile: (408) 975-7501